

We claim:

1. A communications interface comprising:

a plurality of data ports for communicating with a plurality of data channels through which said communications interface receives and transmits data;

a single processor port for communicating with a single communications port on a processor through which said communications interface receives and transmits data;

a memory;

an interface controller for controlling said data as it passes through said communications interface on a receive path from said plurality of data ports to said single processor port and on a transmit path from said single processor port to said plurality of data ports, said interface controller adapted to use said memory to buffer said data; and

one or more channel identifier units adapted to, either individually or in combination, (i) add a channel identifier, which identifies to which data channel said data relates, to said data on said receive path, and (ii) remove a channel identifier from said data on said transmit path.

2. The communications interface according to claim 1, wherein said channel identifier comprises a unique designator assigned to each channel of said plurality of data channels.

3. The communications interface according to claim 1, wherein said interface controller and said one or more channel identifier units comprise a field programmable gate array.

4. The communications interface according to claim 1, wherein said memory is divided into a plurality of memory blocks for each of said plurality of data channels and wherein said interface controller buffers said data in a memory block according to a data channel to which said data relates.

5. A communications interface comprising:

2 a plurality of data ports for receiving data from a plurality of data channels;
3 a single processor port for communicating with a single communications port on a
4 processor;
5 a memory;
6 an interface controller for (i) storing data received by said data ports in said memory
7 in predetermined memory blocks dependent upon the channel from which said
8 received data is received, (ii) accessing said received data from said memory, and
9 (iii) sending said received data to said single processor port on said processor; and
10 a channel identifier insertion unit for adding a channel identifier to said received data
11 prior to said received data leaving said single processor port.

1 6. The communications interface according to claim 5, further comprising a framer unit for
2 parsing data received by any given data port into messages.

1 7. The communications interface according to claim 6, wherein said channel identifier
2 insertion unit is for adding a channel identifier into each of said messages.

1 8. The communications interface according to claim 6, wherein each said message is
2 enveloped by flags and wherein said framer unit is also for stripping said flags.

1 9. The communications interface according to claim 6, wherein each said message is a
2 High-level Data Link Control (HDLC) frame and said channel identifier insertion unit is
3 for adding a channel identifier into a header of each said HDLC frame.

1 10. The communications interface according to claim 6, wherein said message includes an
2 error checking code and said channel identifier insertion unit adjusts said error checking
3 code to account for the insertion of the channel identifier.

1 11. The communications interface according to claim 5, wherein said channel identifier
2 comprises a unique designator assigned to each data channel of said plurality of data
3 channels.

1 12. The communications interface according to claim 5, wherein said interface controller is
2 also for receiving processed data from said single processor port, said processed data
3 including a channel identifier, and said communications interface further comprising:

4 a channel identifier removal unit communicating with said interface controller for
5 removing said channel identifier from said processed data and for communicating
6 said channel identifier to said interface controller,

7 and wherein said interface controller is also for (i) storing said processed data in said
8 memory in a predetermined memory block dependent upon said channel identifier
9 received from said channel identifier removal unit, (ii) accessing said processed data
10 from said memory, and (iii) sending said processed data to a data port of said
11 plurality of data ports dependent upon the memory block from which said processed
12 data was accessed.

1 13. The communications interface according to claim 12, further comprising a framer unit
2 for parsing data received from said single processor port into messages.

1 14. The communications interface according to claim 13, wherein said message includes an
2 error checking code and said channel identifier removal unit adjusts said error checking
3 code to account for the removal of the channel identifier.

1 15. A communications interface comprising:

2 a single processor port for communicating with a single communications port on a
3 processor and receiving data that includes a channel identifier;

4 a plurality of data ports for communicating with a plurality of data channels;

5 a memory;

6 an interface controller for (i) storing data received by said processor port in said
7 memory in predetermined memory blocks dependent upon the channel identifier, (ii)
8 accessing said received data from said memory, and (iii) sending said received data

9 to a data port of said plurality of data ports dependent upon the memory block from
10 which said processed data was accessed; and

11 a channel identifier removal unit for removing a channel identifier from said received
12 data prior to said received data leaving said data port.

1 16. The communications interface according to claim 15, wherein said channel identifier
2 removal unit is adapted to remove said channel identifier prior to said storing said data.

1 17. A communication processing system comprising:

2 a processor having a single communications port; and

3 a communications interface in communication with said single communications port
4 on said processor, said communications interface comprising:

5 a plurality of data ports for communicating with a plurality of data channels
6 through which data is received and transmitted;

7 a single processor port for communicating with said single communications
8 port on said processor;

9 a memory;

10 an interface controller for controlling said data as it passes through said
11 communications interface on a receive path from said plurality of data ports
12 to said single processor port and on a transmit path from said single processor
13 port to said plurality of data ports, said interface controller adapted to use said
14 memory to buffer said data; and

15 one or more channel identifier units adapted to, either individually or in
16 combination, (i) add a channel identifier, which identifies to which data
17 channel said data relates, to said data on said receive path, and (ii) remove a
18 channel identifier from said data on said transmit path.

1 18. The communications interface according to claim 17, wherein said channel identifier
2 comprises a unique designator assigned to each data channel of said plurality of data
3 channels.

1 19. The communications interface according to claim 17, wherein said memory is divided
2 into a plurality of memory blocks for each of said plurality of data channels and wherein
3 said interface controller buffers said data in a memory block according to a data channel
4 to which said data relates.

1 20. A communications interface comprising:

2 a plurality of data ports for communicating with a plurality of data channels through
3 which said communications interface receives and transmits data;

4 a single processor port for communicating with a single communications port on a
5 processor through which said communications interface receives and transmits data;

6 a memory;

7 interface controller means for controlling said data as it passes through said
8 communications interface on a receive path from said plurality of data ports to said
9 single processor port and on a transmit path from said single processor port to said
10 plurality of data ports, said interface controller adapted to use said memory to buffer
11 said data; and

12 channel identifier means for (i) adding a channel identifier, which identifies to which
13 data channel said data relates, to said data on said receive path, and (ii) removing a
14 channel identifier from said data on said transmit path.

1 21. A method for communicating data between a plurality of data channels and a single
2 communications port on a processor, said method comprising:

3 buffering said data in a memory;

4 adding a channel identifier, which identifies to which data channel said data relates,
5 to said data on a receive path between said plurality of data channels and said single
6 communications port; and

7 removing a channel identifier from said data on a transmit path between said single
8 processor port and said plurality of data channels.

1 22. A communications interface comprising:

2 a plurality of data ports for communicating with a plurality of data channels;

3 a plurality of channel identifier insertion units in communication with said plurality
4 of data ports for receiving data and for adding a channel identifier into said data to
5 provide channel-added data;

6 a single processor port for communicating with a single communications port on a
7 processor;

8 a channel identifier removal unit in communication with said single processor port
9 for receiving channel-added data from said single processor port and for removing a
10 channel identifier from said data to provide transmit data;

11 a memory divided into memory blocks for channel-added data and transmit data for
12 each of said plurality of data channels; and

13 an interface controller, in communication with:

14 (a) said plurality of channel identifier insertion units, for (i) storing said
15 channel-added data in said memory in predetermined memory blocks
16 dependent upon the data channel from which the data was received, (ii)
17 accessing said channel-added data from said memory, and (iii) sending
18 said received data to said single processor port; and

19 (b) said channel identifier removal unit, for (i) storing said transmit data in
20 said memory in predetermined memory blocks dependent upon a channel
21 identifier removed by said channel identifier removal unit, (ii) accessing

22 said transmit data from said memory, and (iii) sending said transmit data
23 to a data port of said plurality of data ports dependent upon the memory
24 block from which said processed data was accessed.